A HIGH CAPACITY DATA RECORDING DEVICE BASED ON A DIGITAL AUDIO PROCESSOR AND A VIDEO CASSETTE RECORDER

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ABSTRACT A modified digital audio processor, a video cassette recorder, and some simple added circuitry are assembled into a recording device of high capacity. The unit converts two analog channels into digital form at 44-kHz sampling rate and stores the information in digital form in a common video cassette. Bandwidth of each channel is from direct current to ~20 kHz and the dynamic range is close to 90 dB. The total storage capacity in a 3-h video cassette is 2 Gbytes. The information can be retrieved in analog or digital form.

INTRODUCTION

With the advent of the patch clamp technique the recording of continuous data is now a common need in many laboratories. Unfortunately, this is often not practical with small computer systems because the amount of storage required is beyond the usual capabilities of even large Winchester-type disk drives. Even in the case of large magnetic disks there is the extra complication that the data stored must be transferred to another large capacity medium before another set of data can be taken. The alternative is to use analog instrumentation tape recorders to collect the data and subsequently transfer sections of the data via analog-to-digital (A/D) conversion to the computer for analysis. Analog frequency modulation (FM) tape recorders have quite a limited dynamic range and signal-to-noise ratio and are expensive.

This communication presents a set of simple modifications that allow the use of commercial digital audio processors (DAP) and video cassette recorders (VCR) to record data continuously with digital storage. The system has a capability to record two channels at a sampling frequency of 44 kHz each giving an effective bandwidth of 20 kHz, a dynamic range of ~90 dB, and a recording time of ~3 h per cassette. (Using an L-750 cassette the total recording time is 3 h at speed beta-II and gives a total storage of 2 Gbytes.) The system can be used as a stand alone machine that allows the reproduction of the signal in analog form; in addition, digital outputs are available to play back the information directly into a digital input of a computer for subsequent analysis.

DESCRIPTION

DAPs are used in the audio industry to transform audio signals into digital form in a format compatible with the recording scheme of VCRs. They have two channels and often they have a high (microphone) sensitivity and lower sensitivity (line) inputs with typically a frequency response from 5 to 20,000 Hz. Both channels are digitized with A/D converters and the digital signals are combined in serial form into a stream of data plus error correction words. The stream of data is stored in a memory and the order is scrambled in a predetermined way before being transformed into video format to be sent to the VCR. The idea of the scrambling is to decrease the probability that a dropout in the tape (defect in the surface coating) could affect two consecutive words of information. A large fraction of the errors can be corrected by the built-in error detection and correction during playback, but if the correction is impossible, a linear interpolation is done with the preceding and the next word to the one lost. The output signal from the DAP simulates a video signal of normal television standard; that is, it contains synchronization pulses before each TV line and before each TV field (a field is a half frame) and in between synchronization pulses the video information consists of the ones and zeroes of the digital information as high or low level of the output voltage. In fact, the video output from the DAP can be observed in a TV monitor (or using the VCR, in a regular TV receiver) as a pattern of small rectangles of black and white representing the ones and zeroes of the input signal. The video signal from the DAP is recorded by the VCR in

magnetic tape contained in the cassette as if it were regular TV information. During playback, the output of the VCR is fed back into the video input of the DAP, which takes the digital information contained in the video signal, stores it in a memory, checks for errors, corrects them, and unscrambles the data. The digital stream of data is fed to internal D/A converters whose outputs are available to the user to retrieve the recorded signal in analog form.

The combination of the DAP and the VCR are completely self-sufficient and they do not need any external equipment or internal modifications if one is interested in the recording of audio signals. To use the combination as an instrumentation tape recorder it is necessary to modify the DAP to extend the bandwidth to zero frequency (DC) and improve the frequency response characteristics to use the recorder for time domain applications.

We have modified the DAP (DMP-100; Nakamichi USA Corp., Santa Monica, CA), which has internal 16 bit A/D converters and has separate pathways for input and output. The modifications outlined here are applicable to this unit, the Sony PCM F-1 and the Sony PCM 701-ES (Sony Corp. of America, Park Ridge, NJ), and they may serve as a guide for the modifications of other units available commercially.

Fig. 1 shows a block diagram of the system. It consists of the DAP, the VCR, and a box containing the output stage. The input stage of the DAP must be modified to extend the response to DC, and the digital output must be fetched from the unit to feed the output stage pictured at the left of Fig. 1. The physical arrangement is not critical but, as there is very little space in the DMP-100 DAP, the extra circuitry should be built in a separate box. The analog inputs can go directly into the modified DMP-100 DAP or the new box can be used as a relay box to pass the connections to the DAP by using one multiple pin connector such as a DB25-type connector. Care should be exercised not to mix grounds of the digital and analog lines and shield the analog signals as well as use twisted pairs for the digital lines. The output stage also provides a parallel digital output with clock pulses to be used as a source to a digital computer.

The Input Stage

Fig. 2 *a* shows part of the analog board of the DMP-100 DAP where it can be seen that blocking capacitors are cutting off the low frequencies. (For complete diagrams consult the Sony service manual for the PCM-F1. Also note that the PCM-F1 after serial #800521 and the 701-ES do not have the blocking capacitors in that location, therefore the shorting described below is not needed in those units.) In Fig. 2 *b*, it is shown the modifications to the diagram of Fig. 2 *a* to extend the input frequency response down to DC. The buffer amplifier (IC102 and IC202) was modified to have a gain of one that gives an input range of ±4 V but the user may change that according to the required input range. In any case, it is recommended to keep this buffer as the input stage to decrease noise pick-up. The output of the buffer amplifiers are connected directly to R133 and R233 short circuiting the capacitors. Notice that with this configuration the unit will not have an input filter and it must be provided externally by the user to prevent aliasing during sampling. The filters in the unit are not linear-phase type and they oscillate when the input is a step function and for this reason they have been eliminated from the circuitry. The modification of Fig. 2 can be easily implemented by cutting a few lines in the printed circuit board and adding two shielded cables that can be run on the external face of the printed circuit board to the back of the unit and connected to three pins of a

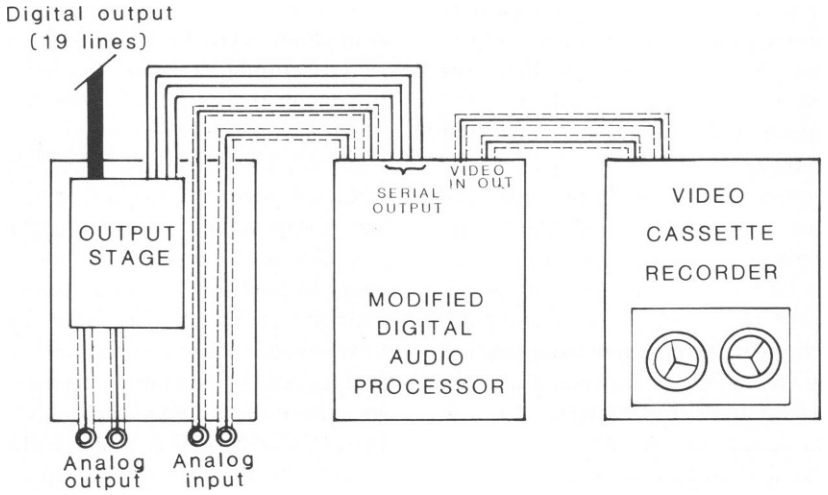

FIGURE 1 Block diagram of the recording system. The *right* unit is a standard VCR, the unit in the *center* is a modified DAP, and the unit at the *left* is the output stage described in the text. The analog inputs are connected via shielded cables through the left unit to the modified DAP. The digital signals from the DAP are connected to the output stage to generate the analog and digital outputs. The digital output consists of 16 data lines and three synchronizing clocks. The DAP is interconnected with the VCR via shielded cables.

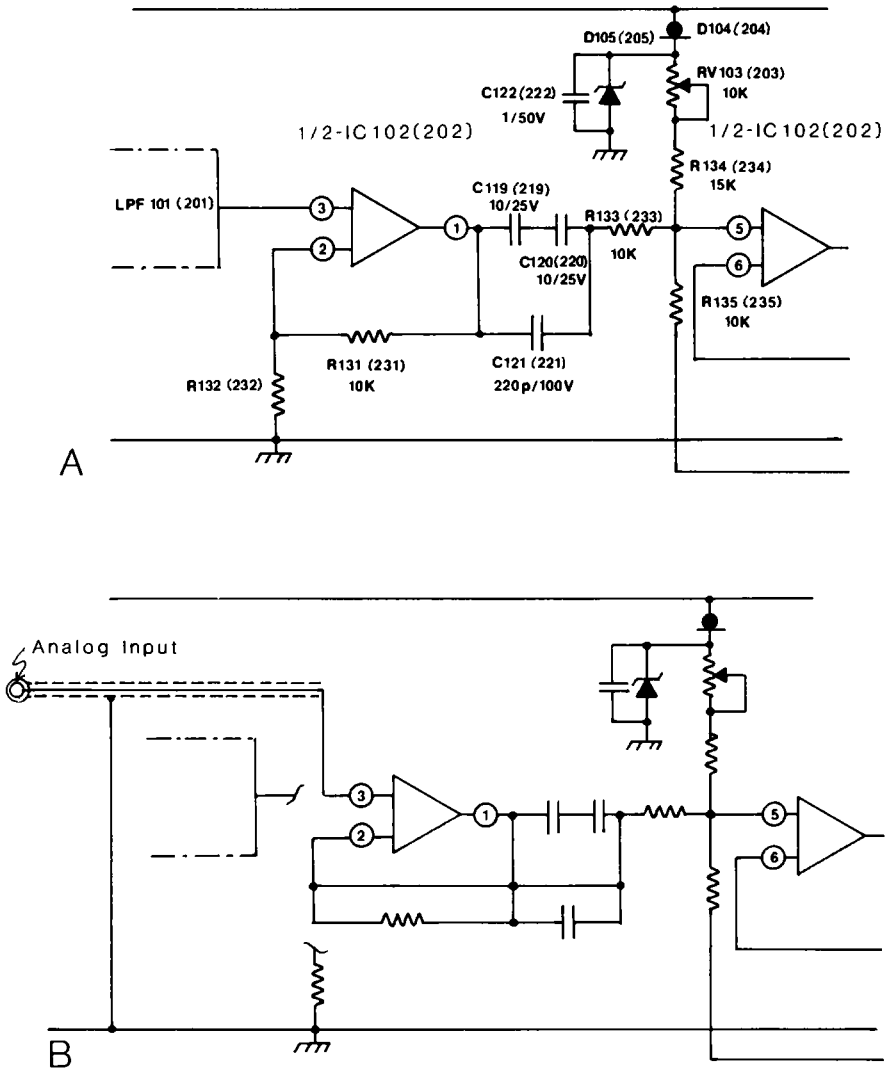

FIGURE 2 Modification of the input stage of the DAP. Most of the analog circuitry is bypassed and the input is done at the level of the buffer preceding the sample and hold switch. (*A*) This represents the circuitry associated with *IC102* of the DMP-100 DAP. The numbers in parenthesis differing by the first digit correspond to the other channel in the unit and the modifications must be made in both channels. (*B*) Same as part *A* but modified. Notice that two cuts must be made in the printed circuit board, two shorting wires installed, and a shielded cable must be connected to the positive input of *IC102* and *IC202*. Note that in the Sony PCM 701-ES and the Sony PCM-F1 (Sony Corp. of America) after serial #800521 the blocking capacitors *C120* (*220*), *C121* (*221*) are not located in the indicated position rendering the shorting unnecessary.

DB25-type connector, which may be installed in the back panel of the unit.

The Output Stage

The analog part of the output stage of the DMP-100 DAP contains only one D/A converter and can be improved substantially by the modification described below which also provides digital lines to feed a computer.

The processed digital output of the DMP-100 DAP is in serial form. To reconstruct the parallel words for both channels one requires the serial data, the word clock, and the bit clock. These signals are available from the integrated circuit labeled IC532 in the digital board of the DMP-100 DAP. The data (DA) is obtained from pin 3 of IC532, the word clock (WCK) from pin 8, and the bit clock (BCK) from pin 6. These three signals are obtained from the digital board of the unit (the board on the bottom of the DMP-100 DAP) and they should be soldered to the pins with twisted pair wires that can be run on the surface of the board and soldered to the same DB25 connector suggested to be installed on the back of the unit. The ground of the digital signals should not be tied to the ground of the input signals.

The schematics of Fig. 3 shows the conversion of the serial signal to parallel form and to analog form. The DA, WCK, and BCK signals from the DMP-100 DAP span from 0 to −5 V and they are first converted to transistor-

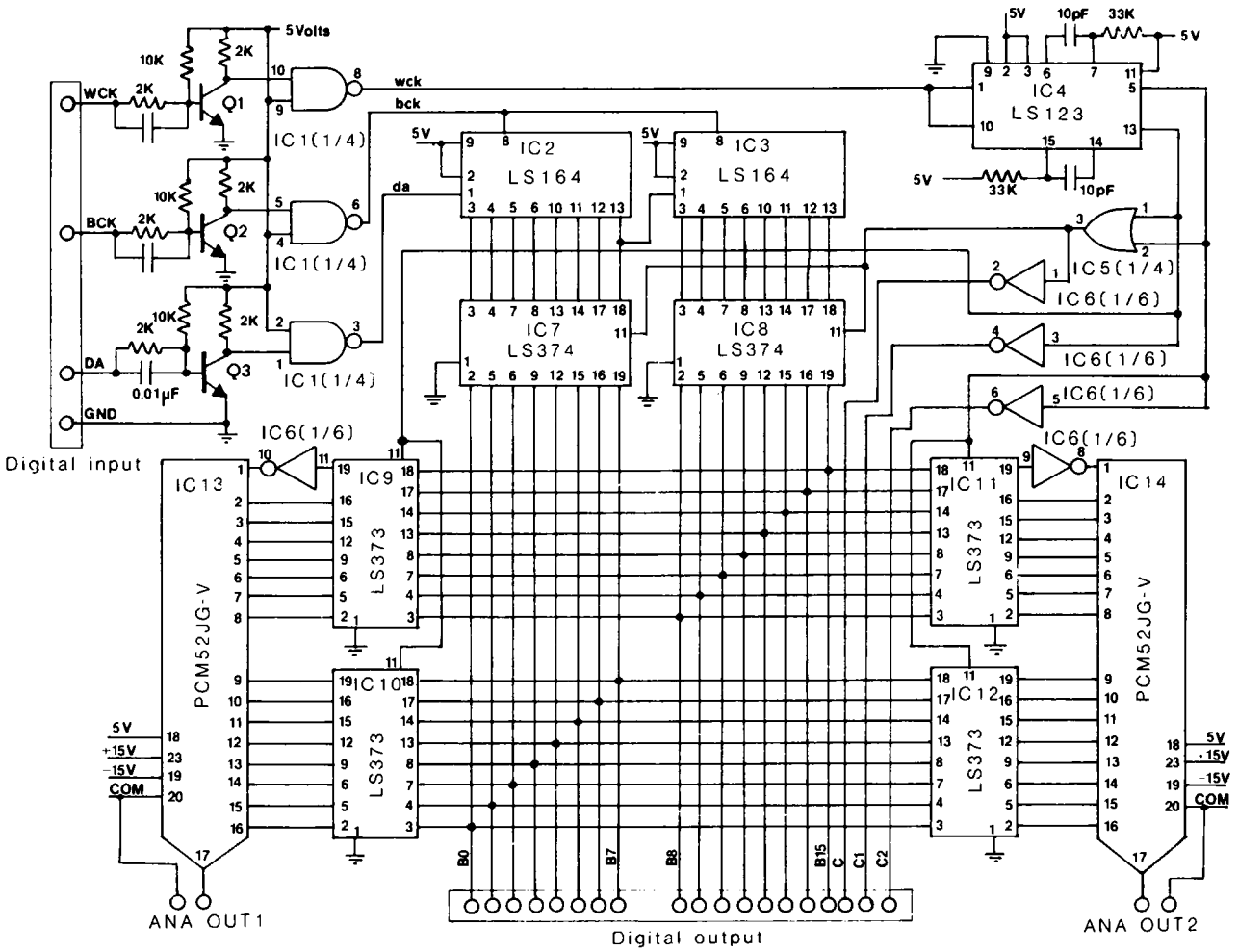

FIGURE 3 Schematic diagram of the output stage. The long rectangle at the left containing four contacts corresponds the the DB25 connector referred to in the text. The rectangle at the bottom of the figure is the Amphenol 50 pin connector explained in the text. This stage requires a 5 V and a ±15 V supplies. *COM* is the common of the ±15 V supply. The digital ground (*GND*) should be tied at only one point with *COM* and bypass capacitors should be connected across the supply inputs of the D/A converters. *B0* through *B15* represent the output bits from least significant to most significant. *C* is the clock for both channels, *C1* and *C2* are the clocks for separate channel transfer. *IC1* is a quad *NAND* gate (*LS00*), *IC5* is a quad *OR* gate (*LS32*), and *IC6* is a hex inverter (*LS04*). *Q1*, *Q2*, and *Q3* are NPN switching transistors such as 2N3904. *ANA OUT1* and *ANA OUT2* are the analog outputs. The inverters connecting *IC9* with *IC13* and *IC11* with *IC14* are used to convert the digital word to complementary offset binary used by the D/A converters.

transistor logic (TTL) levels into DA, WCK, and BCK, respectively, by the transistors pictured in Fig. 3. The BCK is used to clock the shift registers (LS164's) that are fed with the serial data (DA). The leading and falling edges of the word clock (WCK) are used to generate the two synchronizing clocks for each one of the channels by the double one shot LS123. The parallel output of the shift registers is fed to latches (LS374's) that will store each parallel word as is coming out from the DMP-100 DAP. The output of the LS374's can be routed to a multiple pin connector to communicate this unit with a computer. Along with the 16 data bit lines the clocks to synchronize the transfer should go to the same connector. There are three clocks available: C is a clock that synchronizes transfers for both channels and C1 and C2 are clocks that synchronize for only one channel at a time. If transfers are made with C, then right and left channels are both transferred in alternating mode (one word right, one word left, etc.). Using C1 or C2, the transfer is of only one channel while the other is ignored.

The analog output is generated from the parallel output using two 16 bit D/A converters (PCM52JG-V; Burr-Brown Research Corp., Tucson, AZ). Each one of the converters is preceded by its own latch (LS373's) that keeps the digital word present in the input of the converter in between word clocks. The outputs of the converters have a range of ±5 V and to make them equal to the input a 20 KΩ resistor should be installed between pins 17 and 21 of the converter. To smooth the appearance of the output waveforms, the D/A converter outputs should be filtered with a 20-KHz Bessel filter, preferably with six or more poles.

The circuit diagrammed in Fig. 3 may be built in a separate box containing a 5 V and a ±15 V power supply. The back panel may contain a DB25-type connector to receive the digital signals from the DMP-100 DAP and a 50 pin connector (57-40500; Amphenol, Oak Brook, IL) to send the parallel digital output preferably via twisted pairs to a computer. The front panel may contain the analog outputs and, if the analog inputs from the DMP-100 DAP were brought to this box, one may also include the analog inputs. If this option is used, it is important not to interconnect in the box the grounds of the analog input and analog outputs to prevent noise.

We have successfully used this unit together with a VCR (SL-2700 Beta HI-FI; Sony Corp. of America). The Beta HI-FI system has the added advantage that allows the user to have two more channels (AC coupled) that can be used to record synchronizing pulses and voice. Fig. 4 presents the frequency response of the system together with an example of a recorded pulse to illustrate the transient response. The frequency response of the system is essentially that of the Bessel filter used.

In our implementation we have connected the parallel output to a double buffer board installed in the S-100 mother board of a Lomas microcomputer (Lomas Data Products, Westboro, MA). This board is memory mapped and it can be read by the CPU of the computer while the other half is being filled by the DAP and VCR combination. The read information is stored in a Bernoulli-type 10-Mbyte disk (I-Omega model Alpha-10; I-Omega, Ogden, UT) under software control. This arrangement gives more flexibility to the analysis because the retrieval from the disk is easier than from the tape after one has selected an appropriate part of the tape to be analyzed. With the circuitry presented here it is not possible to playback the stored information at slower speeds. If this operation is needed, the transfer to a computer is a necessary step to allow a slower reproduction of the signals (as it may be required in the case of hard copying with an ink writer).

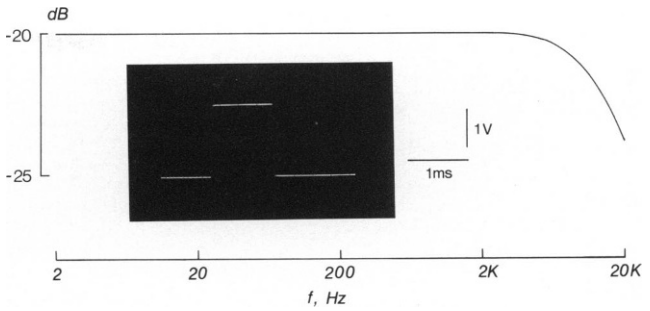

FIGURE 4 Frequency and transient responses of the system. The Bode plot shown was constructed by applying a sinusoidal voltage to the input that was 20 dB below the maximum voltage allowed at the input. The characteristics observed are very close to the response of the filter used in front of the unit (6-pole Bessel-type filter; Frequency Devices Inc., Haverhill, MA) that was tuned for a 20 KHz cut-off. The inset shows the output of the unit for a square pulse of 2-V amplitude. The input range of this prototype was from −10 to +10 V.

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